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Patent
IBM Docket No. FIS920000349US1**REMARKS**

Claims 1 to 15 are pending in the present application. No claims have been amended by this response.

Reconsideration of the Examiner's decisions and reexamination of this application are respectfully requested.

The §103 rejections:

I. Claims 1, 4, 5 and 6 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk U.S. Patent 5,340,437 (hereafter "Erk") in view of Datta et al. U.S. Patent 5,462,638 (hereafter "Datta").

The Examiner has failed to state a prima facie case of obviousness with respect to claims 1, 4, 5 and 6.

The present invention as embodied in claim 1 is directed to the improved uniformity of etching of a film having a plurality of solder bumps. Applicants have found and asserted that this film etches slower at the kerf area of a semiconductor wafer where there are usually no C4 solder structures. (Applicants' specification page 3, lines 21-23 and page 4, line 1). Accordingly, in order to solve this problem first discovered by Applicants, Applicants have proposed rotating the wafer to improve the uniformity of etching. The combination of references proposed by the Examiner do not suggest the problem found by Applicants nor its solution. The Examiner has not addressed this part of Applicants' invention in the Examiner's rejection of claim 1 and thus has failed to consider the subject matter as a whole of Applicants' invention.

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Turning now to the references, Erk is directed to a process wherein a bare silicon wafer, which has been sawed and lapped, is immersed in an etchant bath and then rotated. The etching step is necessary to remove any work damage created by the sawing and lapping and to remove any embedded lapping grit. Among the objects of Erk are to uniformly etch the bare silicon wafer at slow rotation speeds and to have a relatively low total thickness variation across the wafer.

However, the Erk reference is distinguishable on at least three counts from Applicants' invention as embodied in claim 1. The first is that Erk is directed to the etching of bare silicon wafers to remove any residual effects of sawing and lapping. It is to be assumed that as a result of the etching process in Erk, such residual effects would be removed. There is nothing in Erk to indicate that the teachings of Erk would be applicable to any other process other than the removal of such residual effects.

Second, Applicants' claim 1 is directed to a "method of improving the uniformity of etching of a film having a plurality of solder bumps" [emphasis added]. Improving the uniformity of etching is a limitation of Applicants' claim 1. While Erk appears to address thickness variations, both locally and across the entire wafer (col. 2, lines 22-29), this is not the same as uniformly etching a film across the entire wafer as taught by Applicants. That is, Applicants want the same etching in the kerf area and the area with the solder bumps. Since Erk is etching a bare wafer, Erk cannot address this aspect of Applicants' invention.

Third, the teaching of Applicants' invention is that the presence of the solder bumps complicates the etching of the metal films (Applicants' specification page 3, lines 20-21). It cannot be assumed that the etching of a bare wafer as taught by Erk would be applicable to the etching of a wafer with a film having a plurality of solder bumps. Thus, there is no teaching in Erk to indicate that Erk would be applicable to improving the uniformity of etching of a film having a plurality of solder bumps as claimed by Applicants.

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The deficiencies of Erk are not supplied by Datta. Datta is directed to the etching of one of the metallic films (i.e., TiW) underlying the solder bumps and merely teaches, as recognized by the Examiner, that for a semiconductor wafer having solder bumps, the metallic film is conventionally etched by dip etching. There is nothing in Datta to suggest the problem found by Applicants of nonuniform etching. Nor is there anything in Datta to suggest a method of etching by any other method than dip etching in a cassette-type etching process.

The Examiner concludes in the Office Action that "It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to employ any wafer, including a conventional wafer having solder bumps as disclosed by Datta in the process of Erk because Erk does not limit the specific types of wafers processed by the rotating etching process. It would appear that any wafer, including one with solder bumps, would benefit from the uniform etching process of Erk. Applicants have not shown anything unexpected by employing a conventional wafer with solder bumps in a known process for achieving uniform etching."

Applicants disagree with the Examiner's reasoning. As to the first sentence above, the Examiner states that it would have been obvious to combine Erk with Datta "because Erk does not limit the specific types of wafers processed by the rotating etching process." More correctly, since Erk is specifically and only directed to the etching of bare wafers to remove any work damage, there is no teaching in Erk that the process disclosed therein is useful for the etching of any other types of wafers.

As to the second sentence above, where is the teaching in Erk that "It would appear that any wafer... would benefit from the uniform etching process of Erk"? [emphasis added] It is submitted that the Examiner has substituted her opinion for any teaching found in Erk since Erk is specifically and only directed to the etching of bare wafers to remove any work damage.

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As to the third sentence above, Applicants have shown unexpected results in their specification. Depending on the test methodology used, Applicants found improvement of 34% or 78% (page 15, Applicants' specification). Assuming arguendo that the combination of Erk and Datta might result in some improvement in etching, the amount of the improvement found by Applicants would seem to be unexpected.

Any conceivable motivation provided by the Examiner above for the combining of Erk and Datta is negated by the fact that Erk and Datta use different processes and wafers in their respective etching processes.

If modified as suggested by the Examiner above, there would be a different process than that claimed by Applicants since Erk and Datta do not use the same steps and film layer. That is, Erk has no film layer and no solder bumps and immerses and rotates the wafer in an etching bath. Datta, conversely, does have a metallic film layer but etches the wafer in a cassette-type conventional dip etching process. It should be readily apparent that Erk and Datta are directed to two different types of processes with two different kinds of wafers.

Given the flawed reasoning by the Examiner, it is submitted that the Examiner has yet to state a cogent motivation for combining Erk and Datta so as to render obvious Applicants' claim 1.

The Office has the burden under 35 USC §103 to establish a prima facie case of obviousness.

In view of the preceding remarks, it is submitted that the Examiner has failed to carry the Office's burden to state a prima facie case of obviousness with respect to claim 1. Accordingly, claim 1 should be allowable.

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Inasmuch as claims 4 to 6 depend from claim 1, and claim 1 is believed to be allowable, then claims 4 to 6 should be allowable as well. No independent ground of patentability is asserted for claims 4 to 6 at this time.

II. Claims 2 and 3 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta and further in view of Takeshi et al. (English Abstract of JP 9115977 A2) (hereafter "Takeshi"). Claim 7 has been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta and further in view of Barbee et al. U.S. Patent 5,445,705 (hereafter "Barbee").

Inasmuch as claims 2, 3 and 7 depend from claim 1, and claim 1 is believed to be allowable, then claims 2, 3 and 7 should be allowable as well. No independent ground of patentability is asserted for claim 7.

Claims 2 and 3 are believed to be independently patentable.

The Examiner states that Erk in view of Datta fail to teach the step of sequentially rotating the article as claimed in claims 2 and 3. The Examiner further applies Takeshi which reads on rotating the article a predetermined amount but less than a complete rotation and repeating the step of rotating and etching. The Examiner concludes that it would have been obvious to modify Erk and Datta according to Takeshi "for the purpose of improving the method of detecting defects in semiconductor processing."

Erk and Datta have been discussed above. Takeshi discloses an analytical technique for detecting and analyzing so-called flow pattern defects (FPD) in semiconductor wafers. Takeshi is not directed at all to the problem faced by Applicants, to wit, improving the uniformity of a film

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having a plurality of solder bumps. The last statement above by the Examiner is telling. The Examiner has combined Erk, Datta and Takeshi "for the purpose of improving the method of detecting defects in semiconductor processing." That is, the Examiner has combined Erk, Datta and Takeshi to teach a solution to a problem not faced by Applicants. It is submitted that Takeshi is nonanalogous art. In the present case, the reference is directed to a different purpose, as admitted by the Examiner, and so should be considered to be nonanalogous art. Takeshi, then, should be withdrawn as a reference.

Accordingly, with respect to claims 2 and 3, the Examiner has failed to state a prima facie case of obviousness.

III. Claims 8, 11, 12 and 14 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Barbee (?).

While the Examiner has recited Barbee as the secondary reference, it is clear that the Examiner meant to recite Datta as the secondary reference in view of the Examiner's rationale for the rejection of claims 8, 11, 12 and 14.

Therefore, the reasoning recited by Applicants for the allowability of claim 1 is equally applicable here for the allowability of claim 8. That reasoning recited earlier is incorporated by reference herein. Accordingly, claim 8 should be allowable.

Inasmuch as claims 11, 12 and 14 depend from claim 8, and claim 8 is believed to be allowable, then claims 11, 12 and 14 should be allowable as well. No independent ground of patentability is asserted for claims 11, 12 and 14.

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IV. Claims 9 and 10 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Takeshi et al. (English Abstract of JP 9115977 A2). Claim 15 has been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Barbee et al. U.S. Patent 5,445,705.

Inasmuch as claims 9, 10 and 15 depend from claim 8, and claim 8 is believed to be allowable, then claims 9, 10 and 15 should be allowable as well. No independent ground of patentability is asserted for claim 15 at this time.

Claims 9 and 10 are submitted to be independently patentable for substantially the same reasons advanced in favor of claims 2 and 3 and those reasons are incorporated by reference herein.

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IBM Docket No. FIS920000349US1****Summary:**

In view of all of the preceding remarks, it is submitted that claims 1 to 15 are in condition for allowance. If the Examiner finds this application deficient in any respect, the Examiner is invited to telephone the undersigned at the Examiner's earliest convenience to resolve such deficiency.

Respectfully Submitted,
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